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3 **LOGIC SOI STRUCTURE, PROCESS AND**
4 **APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR**

5 **ABSTRACT**

6 A method and structure for forming an emitter in a vertical bipolar
7 transistor includes providing a substrate having a collector layer and a base layer
8 over the collector layer, forming a patterning mask over the collector layer,, and
9 filling openings in the mask with emitter material in a damascene process. The
10 CMOS/vertical bipolar structure has the collector, base regions, and emitter
11 regions vertically disposed on one another, the collector region having a peak
12 dopant concentration adjacent the inter-substrate isolation oxide.